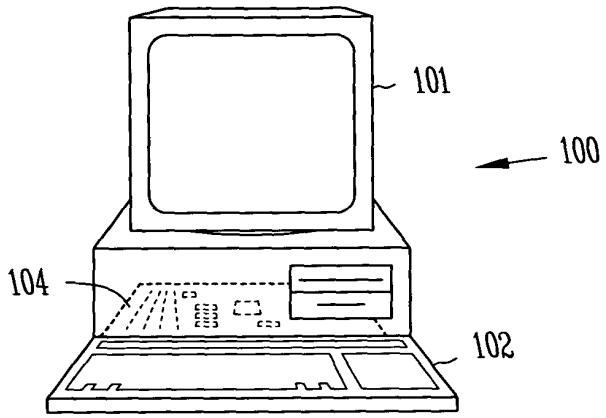
Fig. 1


101
100
104
102

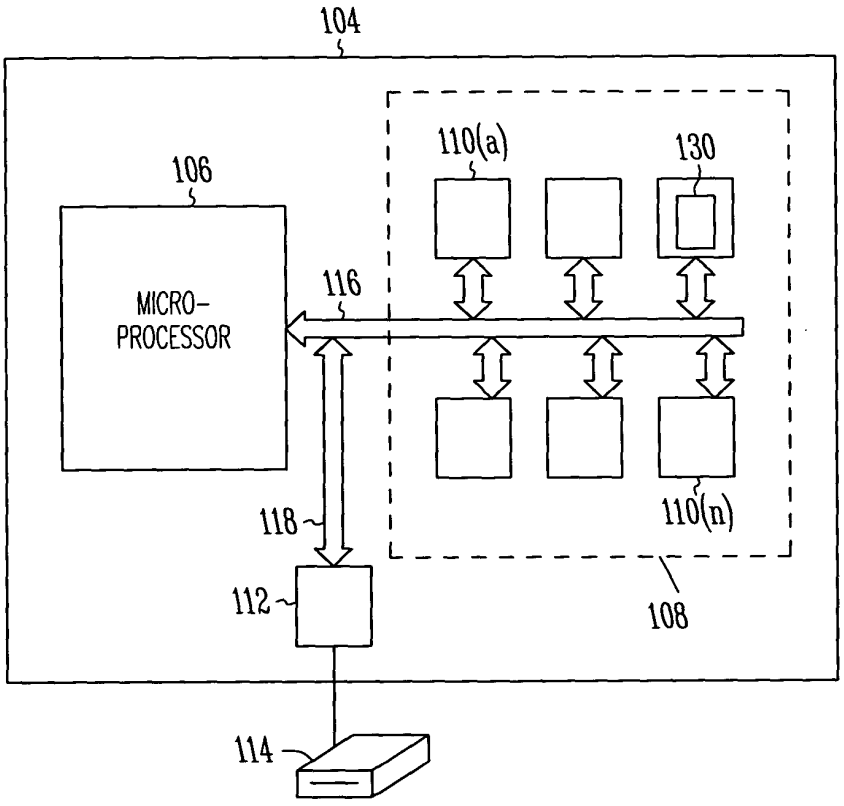

104
106
MICRO-
PROCESSOR
116
110(a)
130
110(n)
118
112
108
114

Fig. 2

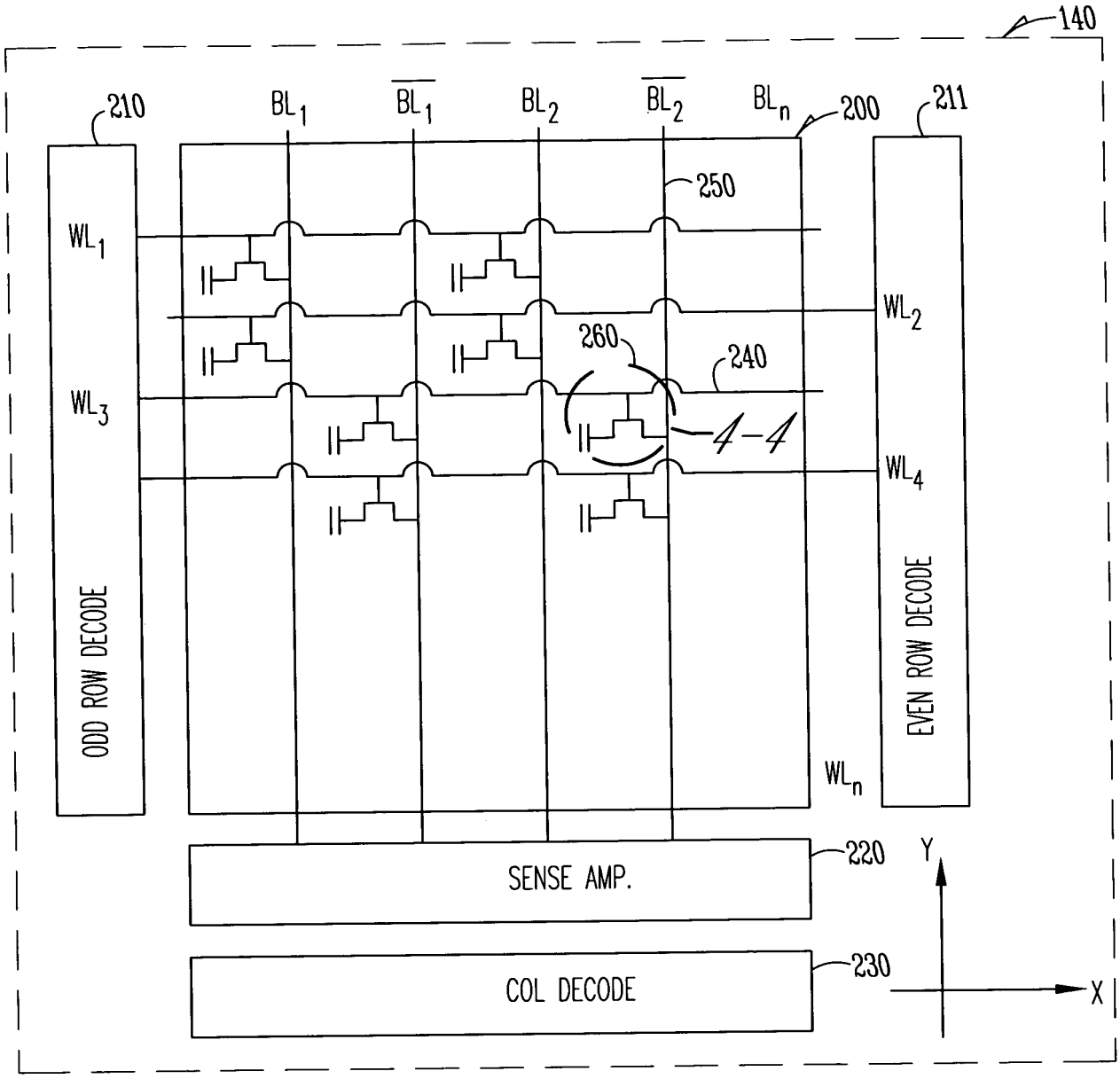

140
210
BL1
BL1
BL2
BL2
BLn
200
211
250
WL1
WL2
260
240
WL3
4-4
WL4
ODD ROW DECODE
EVEN ROW DECODE
WLn
SENSE AMP.
220
Y
230
COL DECODE
X

Fig. 3

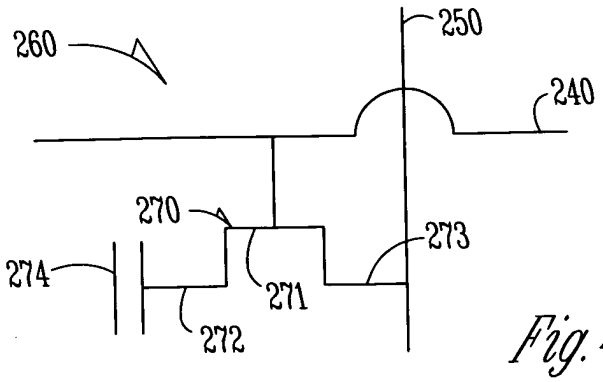

260
250
240
270
273
274
271
272

Fig. 4

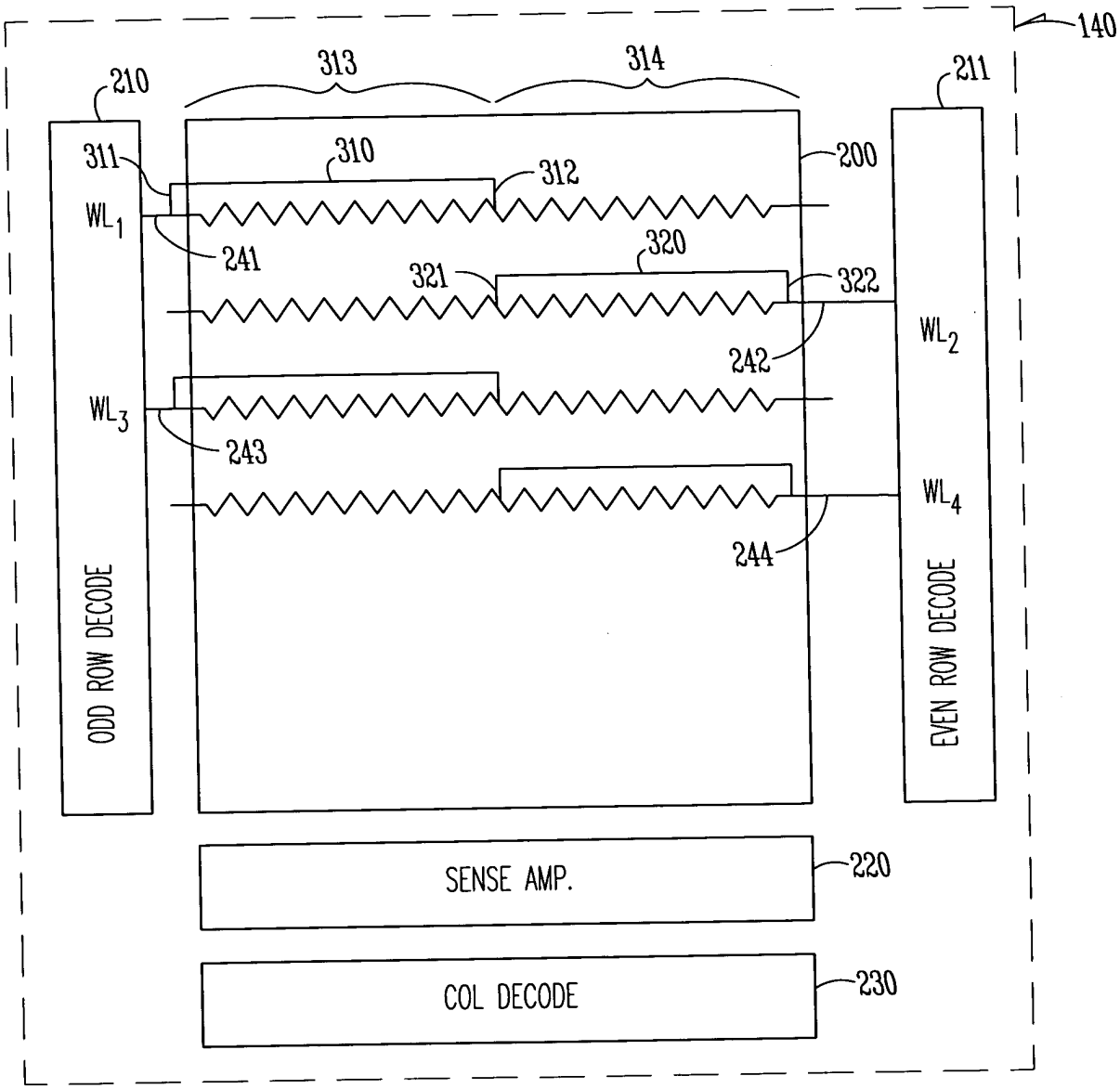

140
210
313
314
211
311
310
312
200
WL1
241
320
321
322
242
WL2
WL3
243
WL4
244
ODD ROW DECODE
EVEN ROW DECODE
SENSE AMP.
220
COL DECODE
230

Fig. 5

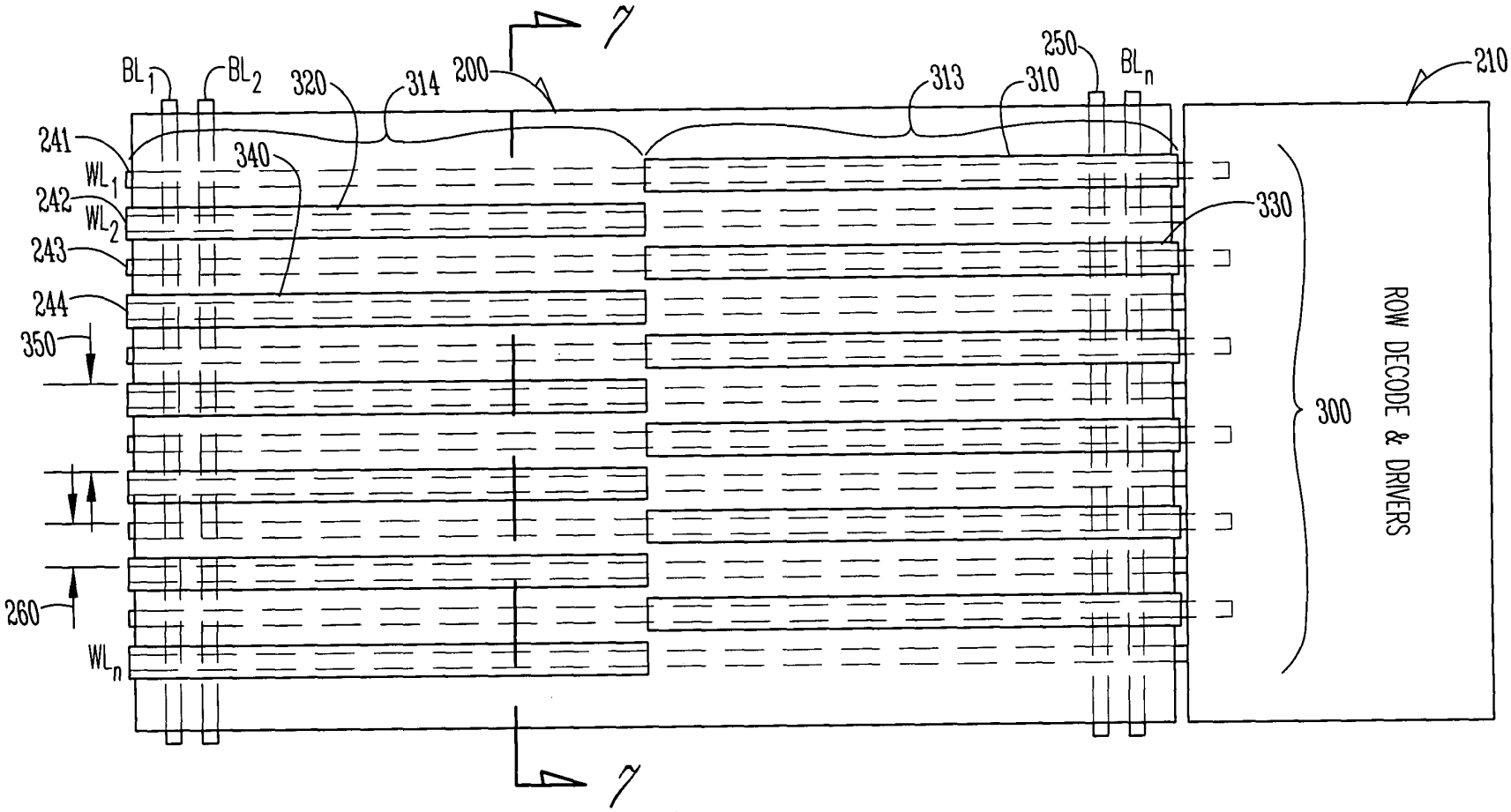

7
BL1
BL2
320
314
200
313
310
250
BLn
210
241
340
WL1
242
WL2
243
244
350
330
ROW DECODE & DRIVERS
300
260
WLn
7

Fig. 6

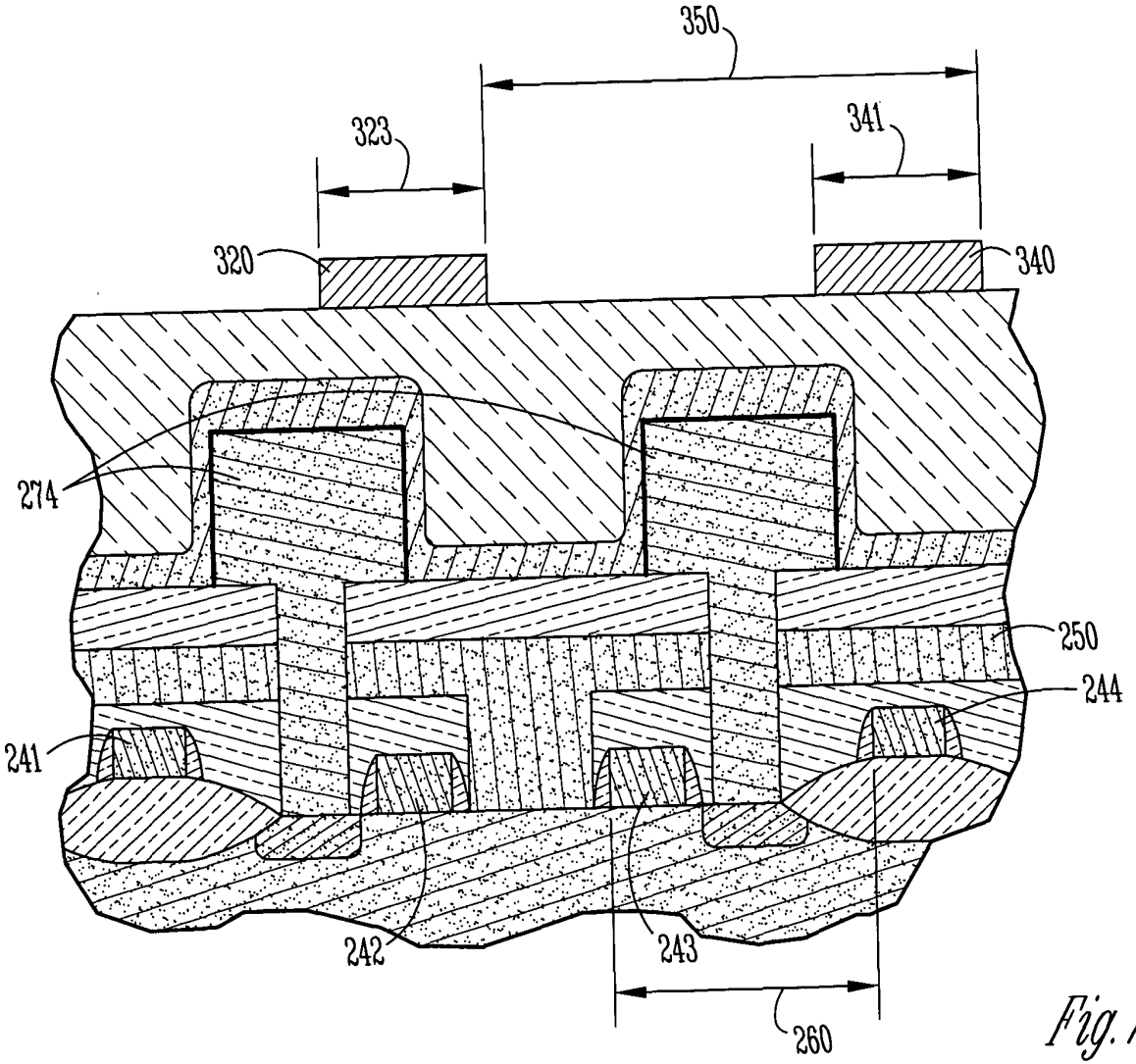


Fig. 7

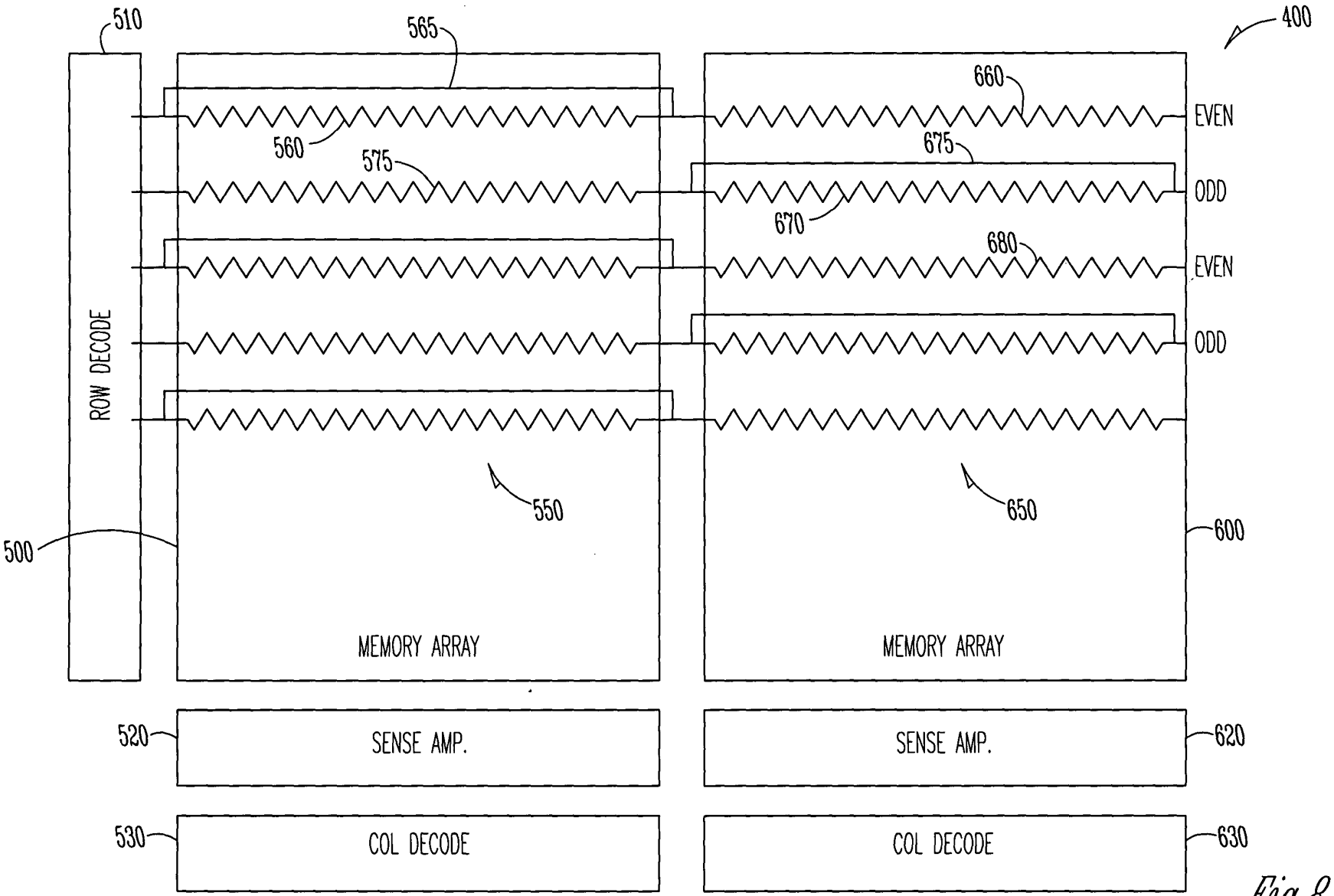


Fig. 8